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QUARTERLY REPORT NO. 10

FOR

ANALOG-TO-DIGITAL CONVERTER

CONTRACT NO. N00014-87-C-0314

1 July 1990—30 September 1990

ARPA Order Number:	9117
Program Code Number:	7220
Amount of Contract:	$3,152,507
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	31 July 1991
Contract Number:	N00014-87-C-0314
Program Manager:	W.R. Wisseman (214) 995-2451
Principal Investigator:	Frank Morris (214) 995-6392
Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 July 1990—30 September 1990

17 October 1990

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter (ADC) and a high-resolution GaAs ADC.

B. ADC Program Overview

The ADC process transfer from TI's CRL development laboratories to the DSEG pilot line is proceeding smoothly. The pilot line completed three ADC lots. The first two lots yielded no functional ADCs but did yield functional DACs. Hughes recently characterized the third lot, and one wafer yielded 45 percent (31 fully functional ADCs from 69 sites). The remaining wafers from this third lot yielded only partially functional ADCs because of high emitter resistance. Process control for the emitter contact metallurgy and threshold control for the n-channel JFETs are the two remaining roadblocks to successful fabrication of the 12-bit ADC scheduled for mask release 4Q90. The Pd/Ge/In n-ohmic contact metal system proposed by S.S. Lau of U.C. San Diego is being evaluated with mixed results. Lot-to-lot variation in contact resistivity is still a problem. The n-channel JFET threshold control depends on the uniformity and repeatability of the epitaxially grown emitter layers. We proposed to Hughes an alternative p-channel JFET in which the threshold control depends on implant dose, energy, and activation level. TI demonstrated this process on a previous IR&D operational amplifier program. The process is totally compatible with the planar overgrowth ADC process, requiring no increase in the number of photomasks compared to the present process. The frequency response of the p-channel JFET should be sufficient to meet the requirements of the 20-Msps 12-bit ADC. Hughes is evaluating the impact of this option.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. ADC Process Status

The DSEG pilot line has started five ADC lots. The first two lots were run to smooth out any processing problems with various splits performed on them. While these first lots did not yield any functional ADCs, they did yield some DACs and, most importantly, provided valuable experience for pilot line personnel. The third lot (Lot 104) yielded HBTs with very high gains

(~1,000); one wafer yielded 45 percent fully functional ADCs and 61 percent DACs. The major yield inhibitors on the third lot were high emitter contact resistance and interlevel leakage. We believe the leakage problem is related to reworking the lot, since the interconnect requirements on the ADC are far less demanding than those on the pilot line MIPS 32-bit microprocessor. The microprocessor has exhibited excellent interconnect and functional yields.

High emitter contact resistances have continued to plague this program. The contact metal system used on Lot 104 is Pd/Ge/Au, which the pilot line established. This process yields contact resistivities in the 1 to 2×10^{-6} ohm-cm^2 range on pilots. However, Lot 104 had a mean contact resistivity in the 5 to 10×10^{-6} ohm-cm^2 range. We are investigating this difference in the results obtained with pilots and actual lots. One theory is that the multiple nitride depositions and strips used throughout the ADC process either damage the GaAs surface or leach out dopant from the surface layer. Photoluminescence measurements compared the surface damage between a control wafer and a wafer with plasma-etched nitride, as would be the case in our n-ohmic process. The measurements detected no difference in surface damage. Lots currently being run in CRL hold the number of times the nitride is stripped and redeposited to a minimum to maintain the surface integrity. No data are available on these lots at this time.

CRL continues to evaluate the Pd/Ge/In contact system proposed by S.S. Lau of U.C. San Diego, with mixed results. For a period of time, the Lau contact system yielded contact resistivities in the mid-10^{-7} range on pilots and occasionally on ADC wafers. During the last 6 to 8 weeks, however, the process yielded results in the high-10^{-6} to mid-10^{-5} range on both pilots and ADC wafers. We analyzed the source materials for Pd, Ge, and In evaporations and found them clean of impurities. Minor differences in the deposition sequence between the S.S. Lau process and our process are now being evaluated. The Lau process uses multiple intermixed layers of evaporated material, while the TI process uses single evaporations of each element. Both processes used essentially the same total metal thickness for each constituent. CRL will attempt to exactly copy the Lau contact recipe.

Throughout the ADC program, the CRL development laboratory has worked with VARO, Inc., of Garland, Texas, to obtain our overgrowth HBT wafers. The DSEG GaAs pilot line is attempting to expand the number of vendors capable of supplying the overgrowth material. Material from Kopin was integrated with material from VARO to form Lot 104. The 45 percent yielding wafer came from VARO, but material from Kopin looks promising. The pilot line will continue this effort. Currently, the pilot line is attempting to obtain overgrowth wafers from Kopin with an ~5 to 10×10^{18} selenium-doped cap layer to improve the emitter ohmic contact resistivity. TI has purchased Morgan Semiconductor, and will evaluate overgrowth material from this source in the future.

The threshold voltage for the n-channel JFETs fabricated in the emitter epitaxial layers have proved difficult to control. The first three pilot-line ADC lots exhibited an enhancement JFET rather than the desired depletion-mode device. An unintentional overetch of the channel region before deposition of the Schottky metal caused this problem. Despite the fact that the current leading lot in the pilot line appears to have good JFETs, concern exists over our ability to control this threshold voltage since funding allows for only two lots of the 12-bit ADC to be fabricated. We are now looking at a fall-back JFET position to enhance the probability of success with these two lots. With minimal frequency requirements for the 12-bit ADC, we are considering a p-channel implanted-channel JFET rather than the n-channel grown-channel JFET. TI developed the p-channel JFET using our ADC overgrowth process during 1988 for an IR&D operational amplifier program. Inclusion of the p-channel JFET requires no increase in the number of masks compared to the existing process, but does require some mask changes. Hughes will evaluate TI SPICE models and decide next month whether to use n-channel or p-channel JFETs.

III. CIRCUIT DESIGN/TESTING

Hughes has completed circuit performance characterization of the latest material from the 12-bit ADC building-block mask set. The mask set contains all the major blocks required in the 12-bit ADC including the sample-and-hold (S/H), gain-switched amplifier, 5-bit quantizer, and 4-bit DAC. The intent of the building-block mask set is to provide circuit performance information that will be folded into the design of the monolithic 12-bit ADC before first mask release.

We evaluated second-lot wafers from the 2-inch wafer research laboratory fabrication line and two lots from the 3-inch wafer pilot fabrication line. Wafer-level testing of the 5-bit ADC included five wafers from the research laboratory and 13 wafers from the pilot line. One wafer from the pilot line yielded fully functional 5-bit ADCs. As shown in Figure 1, the good wafer exhibited 5-bit ADC yield of 45 percent (31 of 69 sites). The remaining 17 wafers yielded only partially functional devices.

Next, we measured I-V characteristics of HBTs and JFETs across five central sites on each of the 18 wafers. No functional JFET devices were found on any wafer. Only one wafer of five from the research laboratory yielded functional HBT devices. Lot 98 from the pilot line (five wafers) yielded functional HBT devices with current gain (β) values ranging from 20 to 50 at 1 mA emitter current on all but one wafer, which produced devices with $\beta > 400$ at 1 mA. These wafers produced only partially functional 5-bit ADCs. In addition, examination of the the 5-bit ADC probe data indicated that high HBT emitter resistance reduced circuit logic swings from 500 mV to less than 20 mV on these wafers. Finally, Lot 104 HBT devices from the pilot line exhibited average β values in excess of 1,000. High emitter resistance and metallization or device shorts resulted in partially functional 5-bit ADCs on all but one wafer that yielded 45 percent.

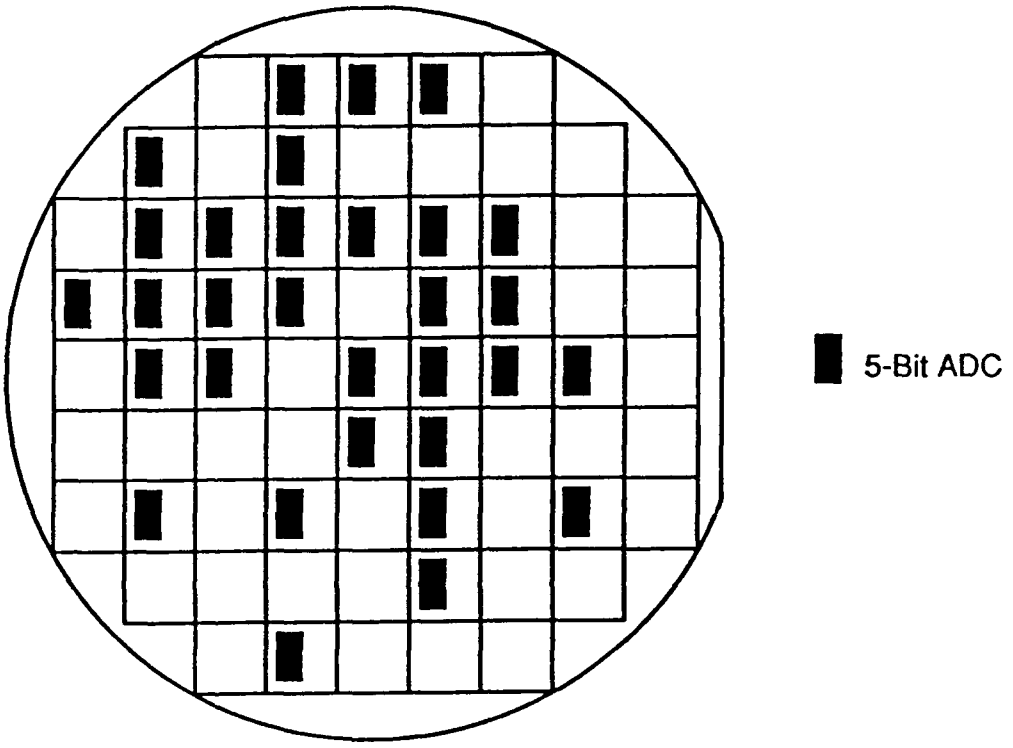

Figure 1. Three-inch HBT pilot line wafer map of fully functional 5-bit ADCs showing 45% yield (ADC104 #2).

Measurement of functional yield and linearity of the 4-bit DAC test cell showed 42 functional DACs of 69 sites, for a yield of 61 percent. Linearity of the DACs ranged between 8 and 16 bits, with a peak distribution centered around 11 bits (Figure 2).

A brief characterization of resistor and transistor current gain provided correlation to measured DAC linearity. We measured a resistor matching pattern consisting of eight series-connected 3-kilohm resistors. Kelvin force and sense/force probe connections eliminated any probe resistance error. As shown in Figure 3, the devices had a mean resistor match of 9.6 bits (0.13 percent) with a one-sigma variation of 2.5 bits, which is sufficient for the 12-bit ADC. Next, a β matching pattern consisting of seven adjacent 5 $\times$ 5 μm emitter transistors was measured, with an emitter current of 2.5 mA per device. As shown in Figure 4, the mean β was 1,350 with a one-sigma variation of 558. The β match data suggest the 4-bit DAC linearity should be centered around 13 bits instead of 11 bits as measured. Further investigation of the 4-bit DAC linearity measurement should resolve the linearity discrepancy.

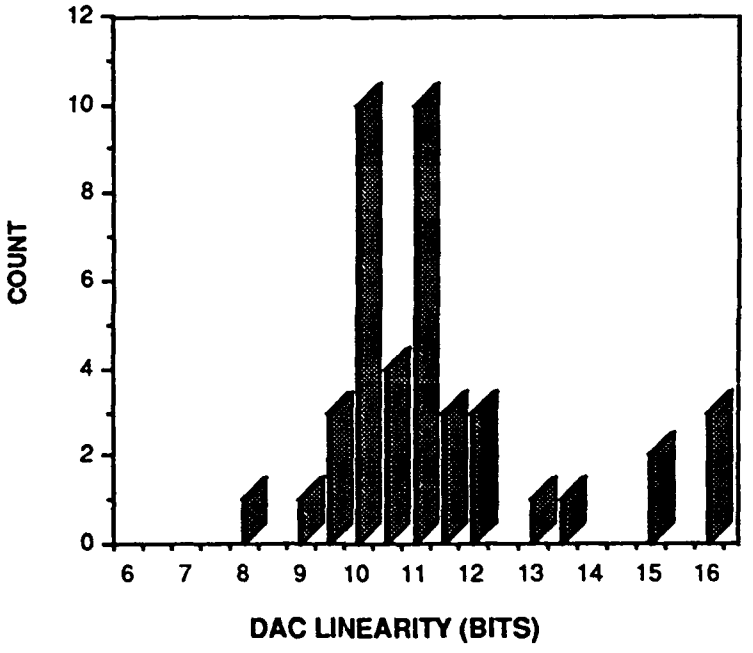

Figure 2. Measured linearity of 4-bit DACs from 3-inch pilot line wafer.

Hughes will continue investigating a p-channel JFET model from TI as an optional high-impedance device for use in the 12-bit ADC design. A decision on the applicability of this device to the 12-bit design will be made next month.

IV. PLANS FOR NEXT QUARTER

- Continue layout of the monolithic 12-bit ADC.
- Complete wafer-level testing of new pilot line wafers.
- Investigate 4-bit DAC linearity measurement.
- Evaluate replacement of n-channel JFET with p-channel JFET.
- Continue to improve n-ohmic contact processes.

W.R. WISSEMAN, Program Manager
System Components Laboratory

PART : HBT16 HBT Acceptance Tests HISTOGRAM
MASK : THB3
LOT : TIHBT06
WAFER : 2

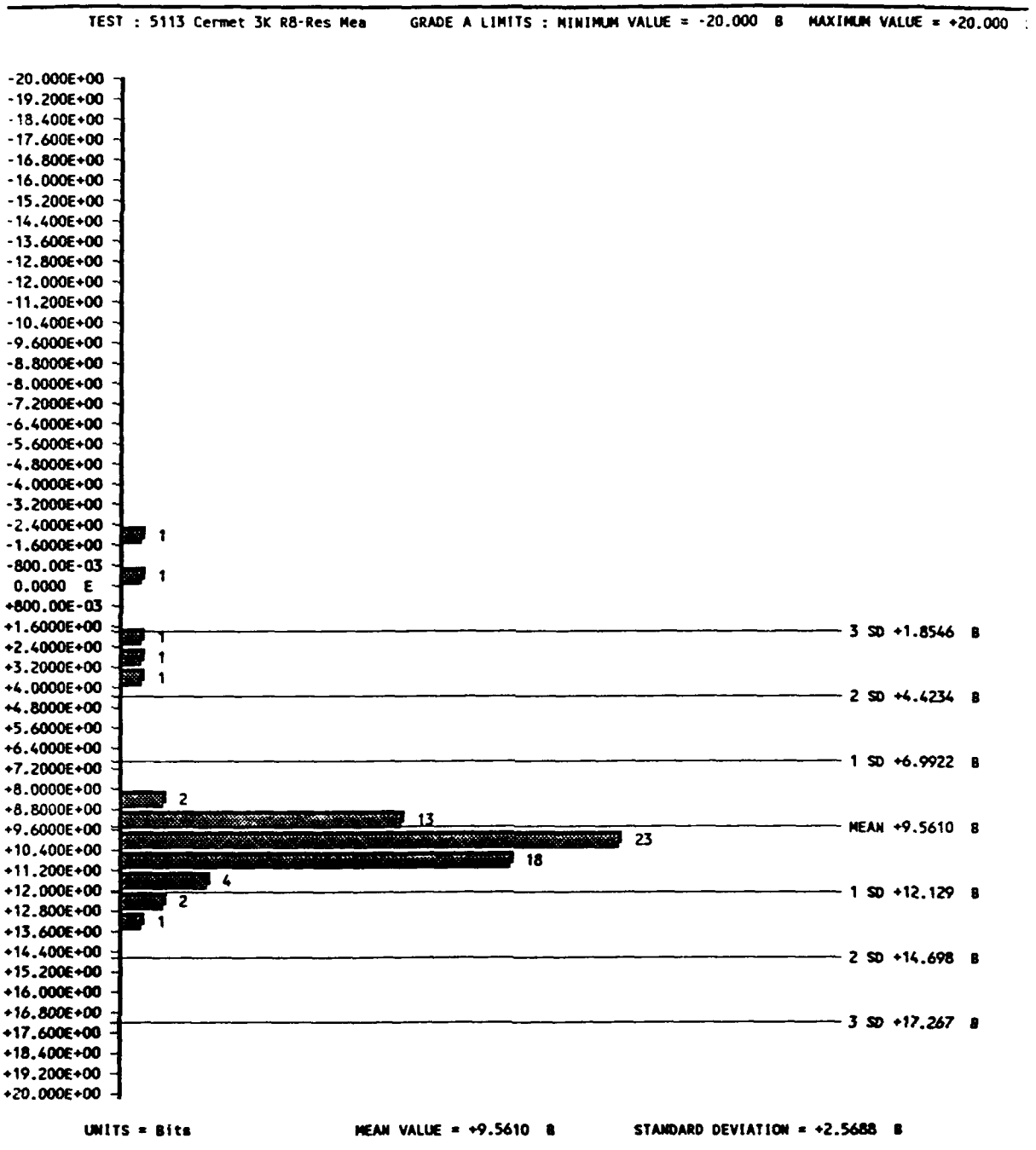

Figure 3. Histogram of 3-kilohm Cermet resistor matching test pattern showing excellent matching of 0.13% (9.6 bits).

PART : HBT16 HBT Acceptance Tests HISTOGRAM
MASK : THB3
LOT : TIHBT06
WAFER : 2

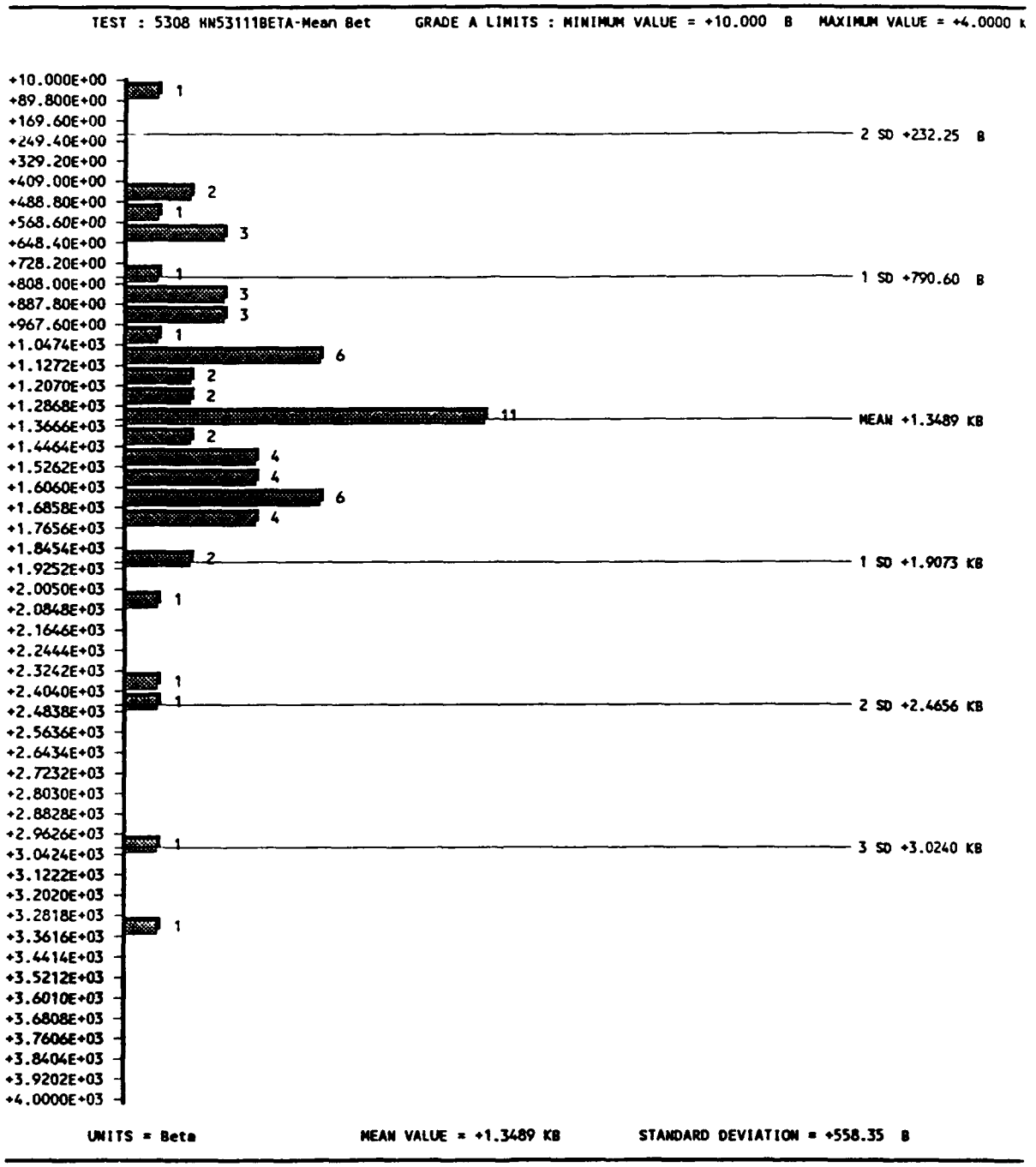

Figure 4. Histogram of 5 × 5 μm emitter current gain matching test pattern.